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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/554,105	08/24/2006	Hiroshi Akahori	46884-5432 (217377)	6588

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EXAMINER	
FLOHRE, JASON A	

ART UNIT	PAPER NUMBER
4112	

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12/24/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/554,105	AKAHORI ET AL.	
	Examiner	Art Unit	
	JASON FLOHRE	4112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/6/08 10/9/08 8/29/08 2/1/08 8/24/08 10/21/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-3 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 2 of copending Application No. 2007/027869. Although the conflicting claims are not identical, they are not patentably distinct from each other see table 1 below.

10554105	**2007027869**
Claim 1	**Claim 1**
energy ray sensitive region	energy ray sensitive region
being formed on front surface side of a semiconductor substrate	semiconductor substrate having (sensitive region must be on front side in order to receive rays)
having a plurality of photoelectric conversion portions that are arrayed two-dimensionally	a plurality of electrodes, each positioned so as to cover a part of said energy ray sensitive region - this with the energy ray sensitive region form the photoelectric conversion portions

generating charges in response to the incidence of energy rays	generates charges in response to the incidence of energy rays
a plurality of transfer electrodes, each being disposed on the front surface side of the energy ray sensitive region with a first direction of the two-dimensional array as the longitudinal direction and transferring the charges in a second direction of the two dimensional array	a plurality of electrodes, each positioned so as to cover a part of said energy ray sensitive region and transferring the charges generated in said energy ray sensitive region to said output section
voltage dividing resistors, disposed in correspondence to the transfer electrodes and each dividing a DC output potential and providing the DC output potential to the corresponding transfer electrode	a voltage dividing circuit electrically connected to each of said electrodes, said voltage dividing circuit including a plurality of voltage dividing resistors serially connected to each other, each of said voltage dividing resistors providing a corresponding DC output voltage from a DC power supply
Claim 2	**Claim 1**
energy ray sensitive region	energy ray sensitive region
being formed on front surface side of a semiconductor substrate	semiconductor substrate having (sensitive region must be on front side in order to receive rays)
having a plurality of photoelectric conversion portions that are arrayed two-dimensionally	a plurality of electrodes, each positioned so as to cover a part of said energy ray sensitive region - this with the energy ray sensitive region form the photoelectric conversion portions
generating charges in response to the incidence of energy rays	generates charges in response to the incidence of energy rays
a plurality of transfer electrodes, each being disposed on the front surface side of the energy ray sensitive region with a first direction of the two-dimensional array as the longitudinal direction and transferring the charges in a second direction of the two dimensional array	a plurality of electrodes, each positioned so as to cover a part of said energy ray sensitive region and transferring the charges generated in said energy ray sensitive region to said output section
wherein a predetermined potential is applied to each of the plurality of transfer electrodes in such a manner that the potential formed under the plurality of transfer electrodes increases gradually in the charge transfer direction	a voltage dividing circuit electrically connected to each of said electrodes, said voltage dividing circuit including a plurality of voltage dividing resistors serially connected to each other, each of said voltage dividing resistors providing a corresponding DC output voltage from a DC power supply
Claim 3	**Claim 1**
a charge accumulation portion, accumulating the charges which have been transferred by a plurality of transfer electrodes, according to each set of the photoelectric conversion portions arrayed in the second direction and outputting the accumulated charges in a batch according to each set of the photoelectric conversion portions	an output section accumulating the charges generated in said energy ray sensitive region, and outputting a current signal or a voltage signal corresponding to the accumulated charge amount

a charge outputting portion, inputting and the successively outputting the charges output from the charge accumulation portions according to each of the sets of the photoelectric conversion portions arrayed in the second direction	an output section accumulating the charges generated in said energy ray sensitive region, and outputting a current signal or a voltage signal corresponding to the accumulated charge amount

Table 1

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Kosonocky (United States Patent 4,646,119), hereinafter referenced as Kosonocky.

Regarding claim 1, Kosonocky discloses charge coupled circuits. Specifically, Kosonocky discloses a substrate (10) formed of n-type silicon (an energy ray sensitive region), which reads on “a solid-state imaging apparatus comprising: an energy ray sensitive region, being formed on a front surface side of a semiconductor substrate, having a plurality of photoelectric conversion portions that are arrayed two-dimensionally, and generating charges in response to the incidence of energy rays”, as disclosed at column 3, lines 37-39 and exhibited in figure 1. Kosonocky also discloses a plurality of transfer electrodes (14-x) located on the silicon-dioxide layer, which reads on “a plurality of transfer electrodes, each being disposed on the front surface side of

the energy sensitive region with a first direction of the two-dimensional array as the longitudinal direction and transferring the charges in a second direction of the two-dimensional array", as disclosed at column 3, lines 48-50 and exhibited in figure 1. Kosonocky discloses that voltage applied to electrode 30-1a may be taken from one point along a voltage divider and the voltage applied to electrode 30-1b may be taken from another point along the voltage divider, which reads on “voltage dividing resistors, disposed in correspondence to the transfer electrodes and each dividing a DC output potential and providing the DC output potential to the corresponding transfer electrode", as disclosed at column 13, lines 61-65 and exhibited in figure 10.

Regarding claim 2, Kosonocky discloses charge coupled circuits. Specifically, Kosonocky discloses a substrate (10) formed of n-type silicon (an energy ray sensitive region), which reads on “a solid-state imaging apparatus comprising: an energy ray sensitive region, being formed on a front surface side of a semiconductor substrate, having a plurality of photoelectric conversion portions that are arrayed two-dimensionally, and generating charges in response to the incidence of energy rays”, as disclosed at column 3, lines 37-39 and exhibited in figure 1. Kosonocky also discloses a plurality of transfer electrodes (14-x) located on the silicon-dioxide layer, which reads on “a plurality of transfer electrodes, each being disposed on the front surface side of the energy sensitive region with a first direction of the two-dimensional array as the longitudinal direction and transferring the charges in a second direction of the two-dimensional array", as disclosed at column 3, lines 48-50 and exhibited in figure 1. Kosonocky further discloses another method of creating asymmetrical depletion zones

comprising two very closely spaced electrodes as 30-1a and 30-1b with a fixed, direct-voltage offset indicated schematically by battery 32, between them, which reads on “wherein a predetermined potential is applied to each of the plurality of transfer electrodes in such a manner that the potential formed under the plurality of transfer electrodes increases gradually in the charge transfer direction”, as disclosed at column 13, lines 53-55 and exhibited in figure 10.

Regarding claim 3, Kosonocky discloses everything claimed as applied above (see claim 1), in addition Kosonocky discloses means C1 including a collector of charge carriers located in the substrate in close proximity to the control plate 14-(n+1), which reads on "a charge accumulation portion, accumulating the charges which have been transferred by a plurality of transfer electrodes, according to each set of the photoelectric conversion portions arrayed in the second direction and outputting the accumulated charges in a batch according to each set of the photoelectric conversion portions”, as disclosed at column 3, lines 53-55 and exhibited in figure 1. Kosonocky further discloses electrodes 17a, 16a-0, 16a-1, and 16a-2 which represent the input end of a shift register for removing the output signal from the system, the shift register reads on “a charge outputting portion, inputting and the successively outputting the charges output from the charge accumulation portions according to each of the sets of the photoelectric conversion portions arrayed in the second direction", as disclosed at column 31, lines 30-32 and exhibited in figure 51.

Regarding claim 4, Kosonocky discloses a plurality of transfer electrodes (14-x) located on the silicon-dioxide layer, which reads on “a solid state imaging apparatus

comprising: a set of transfer electrodes, disposed via an insulating layer on the front surface of a semiconductor substrate and aligned in a single direction", as disclosed at column 3, lines 48-50 and exhibited in figure 1. Kosonocky further discloses that voltage applied to electrode 30-1a may be taken from one point along a voltage divider and the voltage applied to electrode 30-1b may be taken from another point along the voltage divider, which reads on “voltage dividing resistors that electrically connect the respective transfer electrodes”, as disclosed at column 13, lines 61-65 and exhibited in figure 10.

Regarding claim 5, Kosonocky discloses everything as applied above (see claim 4), in addition Kosonocky discloses, that voltage applied to electrode 30-1a may be taken from one point along a voltage divider and the voltage applied to electrode 30-1b may be taken from another point along the voltage divider, which reads on “the voltage dividing resistors divides a DC output voltage from a DC power supply”, as disclosed at column 13, lines 61-65 and exhibited in figure 10.

Regarding claim 6, Kosonocky discloses everything claimed as applied above (see claim 4), in addition Kosonocky discloses means C1 including a collector of charge carriers located in the substrate in close proximity to the control plate 14-(n+1), which reads on "a charge accumulation portion, accumulating the charges which have been transferred by a plurality of transfer electrodes, according to each set of the photoelectric conversion portions arrayed in the second direction and outputting the accumulated charges in a batch according to each set of the photoelectric conversion portions”, as disclosed at column 3, lines 53-55 and exhibited in figure 1. Kosonocky further discloses electrodes 17a, 16a-0, 16a-1, and 16a-2 which represent the input end

of a shift register for removing the output signal from the system, the shift register reads on “a charge outputting portion, inputting and the successively outputting the charges output from the charge accumulation portions according to each of the sets of the photoelectric conversion portions arrayed in the second direction", as disclosed at column 31, lines 30-32 and exhibited in figure 51.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON FLOHRE whose telephone number is (571)270-7238. The examiner can normally be reached on Monday to Thursday 8:00 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Jeffery Harold can be reached on 571-272-7519. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JF
/Jefferey F Harold/
Supervisory Patent Examiner, Art Unit 4112